A 2-W Ku-BAND MONOLITHIC GaAs FET AMPLIFIER*

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ABSTRACT

A monolithic three-stage Ku-band GaAs FET power amplifier has been designed and fabricated. Epitaxial layers are grown by molecular beam epitaxy and FETs have a source overlay geometry with the n^+ ledge channel structure. The amplifiers have up to 2 W output power at 16.5 GHz with 12 dB gain and 20% efficiency.

INTRODUCTION

Monolithic GaAs FET power amplifiers are being developed at several laboratories for phased-array radar and satellite communication applications. The highest power X-band monolithic amplifiers have had output powers at the 2 W level, [1,2] but with only one or two stages of amplification. The highest reported output power from a monolithic amplifier at Ku-band is only about 0.5 W. This was from two very broadband amplifiers, one having a conventional single-ended design,[3] and one a distributed design .[4] The present paper reports a significant increase in output power from a Ku-band monolithic amplifier. Up to 2 W has been obtained at 16.5 GHz with 12 dB gain and 20% efficiency from a three-stage amplifier. The circuit and FET development contributing to this excellent performance are described below.

CIRCUIT DESIGN

The circuit topology of the three-stage amplifier is shown in Figure 1. FET equivalent circuit parameters deduced from S-parameter data were used for the amplifier design. The FET gate widths of the three stages are 1.2 mm, 2.4 mm, and 6.0 mm. The lumped inductors shown in the figure have been replaced by high-impedance (~ 80 ohms) transmission lines on the actual circuit. The use of multiple transmission lines allows for more uniform phase and amplitude distributions to each portion of the FET for minimum gain degradation. Interstage dc blocking capacitors are used as shown in Figure 1. Computer simulations of this amplifier show that a gain of up to 15 dB can be obtained in the 16 to 20 GHz range. The exact center frequency can be determined by the values of the interstage matching (shunt) capacitors and the transmission line lengths.

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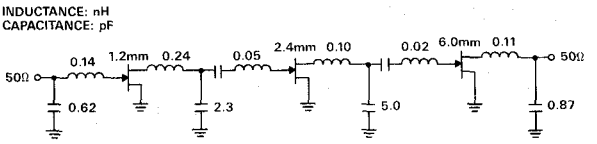

Figure 1 Circuit Topology of the Three-Stage Monolithic Amplifier

FET DESIGN

The achievement of high output power from Ku-band monolithic amplifiers requires very high performance FETs. It is necessary to have low source lead inductance to obtain high gain, but the layout should also be compact to prevent excessive phase difference between different parts of the FET.[5] The source overlay structure with via grounding was chosen as the best FET design for this purpose.[5,6] With this geometry sources are connected by air bridges to large pads on the gate side of the FET that are grounded by vias to the back of the slice. Figure 2 is an SEM photograph of the 1.2 mm gate width first stage FET on an actual circuit (input on the lower left). The large pads in the figure are the grounded source pads (vias not visible). Figure 3 is a closeup photograph showing the air bridges.

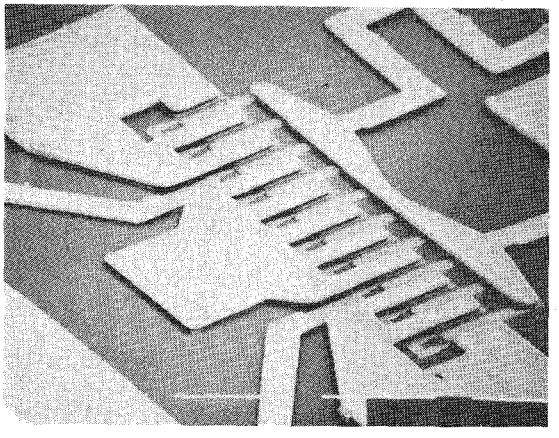

Figure 2 SEM Photograph of the 1.2 mm Gate Width FET on a Monolithic Amplifier

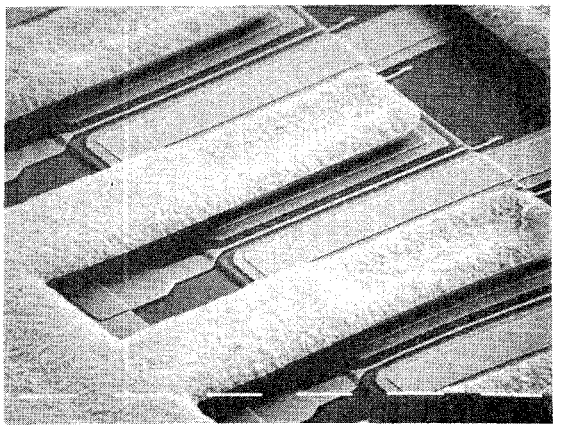

Figure 3 SEM Photograph Showing the Air Bridges

Other FET parameters are chosen as trade-offs between the contradictory requirements of small device size, small temperature rise during operation, high gain, high gate yield, and low attenuation and phase shift of the microwave signal along the gate fingers. For the present application a gate length of 0.5 μm was chosen. The average gate-gate spacing is 25 μm and the gate finger width is 60 μm on the first two FET stages. It was necessary to increase the third stage FET gates to 100 μm in width in order to keep the FET size within reasonable limits.

In addition to the FET geometry, the channel structure has a significant effect on microwave performance. The n+ ledge channel structure[7] sketched in Figure 4 is employed since it has been shown to increase both the gain and output power of high frequency GaAs FETs.[8]

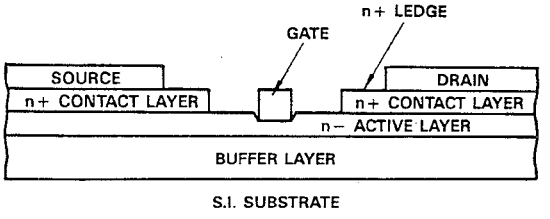

Figure 4 n+ Ledge Channel Structure

CIRCUIT FABRICATION

Figure 5 is a photograph of a portion of a slice following completion of front side processing. Centered in the photograph is a three-stage amplifier (input on the left) having the topology shown in Figure 1. The amplifier, while only 3.3 mm x 2.0 mm x 0.1 mm, contains three source overlay FETs and all series and shunt capacitors and transmission lines. The small input and output shunt capacitors (Figure 1) are realized by the capacitance to ground of the largest pads seen in Figure 5. The other capacitors are of the MIM type with 0.4 μm of silicon nitride as the dielectric. The interstage shunt capacitors have their bottom plates grounded by vias to large pads, similar to the FET grounding vias.

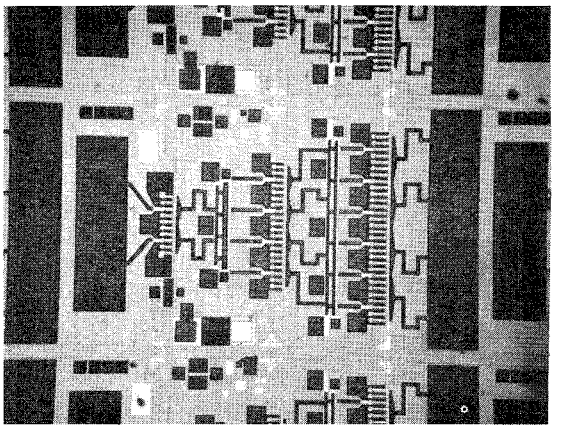

Figure 5 Monolithic Amplifier Slice Following Completion of Front Side Processing

The substrates used in this work are two-inch diameter Cr-doped LEC slices. The epitaxial layers are grown by molecular beam epitaxy (MBE) in a commercial Riber MBE-2300 system.[8] The material structure comprises three epitaxial layers: a 1 μm undoped buffer layer, an 0.3 μm n-GaAs active layer doped to about 2.5 x 10^{17} cm^{-3} with Si, and an 0.2 μm n+ GaAs contact layer doped to about 4 x 10^{18} cm^{-3} with Si. The critical interface between the n layer and the buffer layer has a maximum slope of about 40 nm/decade. The layers are extremely uniform with the best slice having a standard deviation in saturated drain current (I_{sat}) across a two-inch slice of only 16 mA/mm gate width, which is only 0.65% of the mean of 2465 mA/mm gate width. This I_{sat} is so high because it also includes the n+ layer. After gate recess etching and gate metalization, the standard deviation of I_{dss} was 21.5 mA/mm gate width which was 6.2% of the mean of 349 mA/mm gate width. Owing to this high degree of uniformity, there was no loss in circuit yield due to the material.

Following epitaxial layer growth, mesas are etched to isolate FETs and AuGe/Ni/Au ohmic

contacts are formed by lift-off and alloying at 450°C. The wide recess pattern (~ 3 μm wide) of the n+ ledge structure is then defined in PMMA by electron beam lithography and the channel is etched through the n+ layer into the n layer. The 0.5 μm gate pattern is then similarly defined in a new layer of PMMA and the GaAs is etched again down to the final I_{sat} value. The Ti/Pt/Au gates are then produced by evaporation and lift-off. The same set of alignment marks is used for both the wide recess and gate definition. Another Au-based layer is evaporated and lifted off to produce the capacitor bottom plates, inductors and source grounding areas. MIM capacitors are fabricated and plated gold air bridges are formed to contact FET sources and capacitor top plates. The transmission lines and all pads are also plated with ~ 3 μm of gold at the same time. The slices are then lapped to 100 μm and grounding vias are etched by reactive ion etching. A 10 μm thick plated gold heatsink interconnects all the vias.

MICROWAVE PERFORMANCE

The gain-frequency response of the highest power amplifier tested is shown in Figure 6. Two watts output power was measured at 16.5 GHz with 12 dB gain and 20% efficiency. The linear gain was 14 dB at the 1 watt output power level. Another amplifier from the same slice was operated with the third stage sawed off and 1.6 watts was obtained with 9 dB gain and 26% efficiency at the same frequency. This 1.6 watts is an extremely high power for a 2.4 mm gate width FET--a higher power density than the best reported at that frequency from a discrete FET.[6]

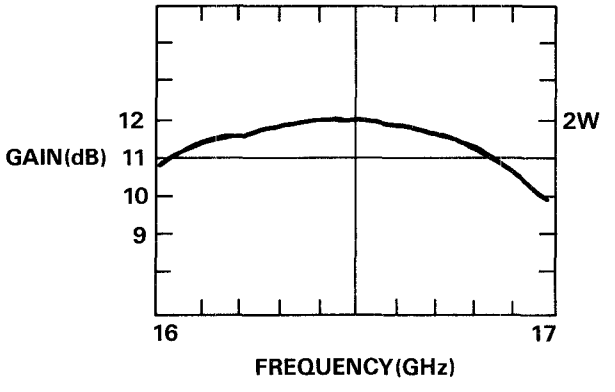

Figure 6 Microwave Performance of a Three-Stage Monolithic Amplifier. RF Input = 21 dBm, V_{ds} = 7.3 V, I_{ds} = 1.27 A, V_g = - 0.9 V

Originally it was thought that the low output power density of the three-stage amplifier relative to the two-stage amplifier was due to non-optimum impedance matching between the second and third stage FETs caused by the distributed nature of the interstage capacitors. However, recent measurements on FETs sawed from all three amplifier stages indicate that a good deal of the problem lies with the third stage FET itself, mainly due to excessive source lead inductance per unit gate width. Although it has 2.5 times the gate width of the second stage FET, it has only two more source grounding vias. It is thought that with a lower source inductance FET design and improved impedance matching between the second and third stage FETs, 2.5 to 3 watts output power will be obtained.

One slice was processed with 0.55 μm silicon nitride capacitor dielectric instead of 0.40 μm in order to shift the operation to higher frequency. Figure 7 shows the gain-frequency response of a three-stage amplifier from this slice. 1.6 watts was obtained at 19 GHz with 9 dB gain.

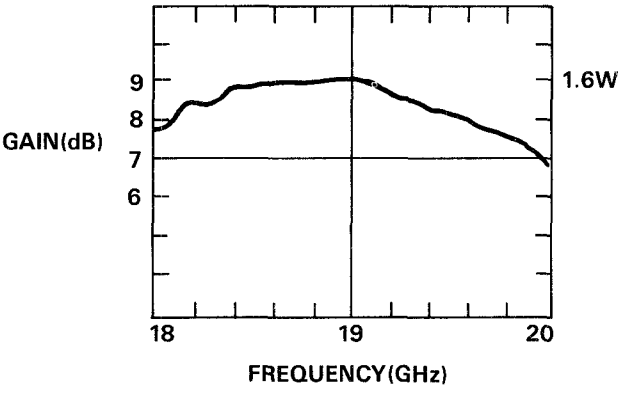

Figure 7 Microwave Performance of a Three-Stage Monolithic Amplifier. RF Input = 23 dBm, V_{ds} = 9 V, I_{ds} = 1.6 A, V_g = - 1.8 V.

CONCLUSIONS

Output powers up to 2 watts have been obtained from a three-stage monolithic amplifier operating at 16.5 GHz. This excellent performance is due to the simple circuit topology, the source overlay FET geometry, the high quality of the MBE material, and the use of the n+ ledge FET channel structure.

ACKNOWLEDGMENTS

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